

IMPROVEMENT OF THE QUALITY FACTOR OF RF INTEGRATED INDUCTORS BY LAYOUT OPTIMIZATION

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ABSTRACT

A systematic method to improve the quality factor of RF integrated inductors is proposed. The method is based on the inductor's layout optimization, and has been successfully applied to the design of square spiral inductors performed using a silicon based MCM technology and silicon micromachining post processing.

INTRODUCTION

One of the key factors which determines the performance of Radio Frequency Integrated Circuits (RFIC's) is the availability of good quality integrated inductors. Unfortunately, parasitic effects, such as coupling capacitance and losses related to the integration substrate, affect these components degrading their performance. These unwanted effects are particularly important using silicon substrates. [1,2]

Recently, the use of silicon micromachining techniques to remove the integration substrate underneath the planar inductors has overcome this problem [3-5]. So, both the inductor Self Resonant Frequency (SRF) and Quality factor increase significantly. However, once the silicon substrate is removed, other factors, which also degrade the inductor's performance, become relevant and must be

taken into account. Among them, magnetically induced currents on the inductor's coil (Eddy currents) [6] could be the most significant. These currents are directly dependent on the time varying magnetic flux through the metal strip used to perform the inductor's spiral. The direct consequences of these currents are frequency dependent losses, which increase as the metal strip width increases.

In the usual case of an spiral inductor performed using a constant width metal strip, the influence of magnetically induced losses is much more important in the inner turns of the coil, where the magnetic field reaches its maximum. According to this, some authors proposed the elimination of the central turns to reduce losses [6]. However, this is not the best procedure to improve the inductor's quality factor.

In this work we propose a systematic method to optimize the inductor's layout in order to reach maximum quality factor. The method is particularly useful when applied to inductors which fabrication process includes silicon substrate removal. However, it is also applicable in the case of low loss integration substrates. The proposed method optimizes the width of the metal strip for each turn of the coil, leading to a variable strip width layout. It has been used to design square spiral inductors in a silicon based MCM technology complemented with silicon micromachining post processing. Comparing the best results

obtained for a single strip width inductor with those of the optimized layout a significant improvement in the quality factor is observed.

DESCRIPTION OF THE METHOD AND RESULTS

The starting point of the proposed method is the analysis of the series resistance of the inductor's coil. This parameter has two main contributions. One of them is related to the ohmic losses. This contribution increases as the width of the metal strip decreases. The other one is related to the magnetically induced losses. This contribution increases as the width of the metal strip increases. According to this, there must be an optimum strip width, which minimize series resistance and then maximize quality factor. Moreover, taking into account the frequency dependence of magnetically induced losses, the optimum strip width will be different for each frequency of operation of the inductor. This behavior is clearly shown on figure 1. In this figure the quality factor of different 20nH inductors are plotted as a function of the metal strip width. These results have been obtained by numerical simulation using the HP Momentum planar solver. In order to reproduce as close as possible the actual inductors the simulation substrate includes the whole set of layers of the available MCM technology. Moreover, to properly take into account magnetically induced effects, an accurate mesh of the inductor's layout has been done. The validity of the simulation procedure has been demonstrated by comparing the results with experimental measurements.

According to the above results, by doing a small number of simulations it is possible to find the strip width which optimize the inductor's quality factor for a given

frequency. However, much better results could be obtained if a different strip width is used for each turn of the coil. So, narrow strips will optimize losses in the inner turns, where magnetic field reach its maximum, while wide strips will optimize the outer turns, where ohmic losses are predominant.

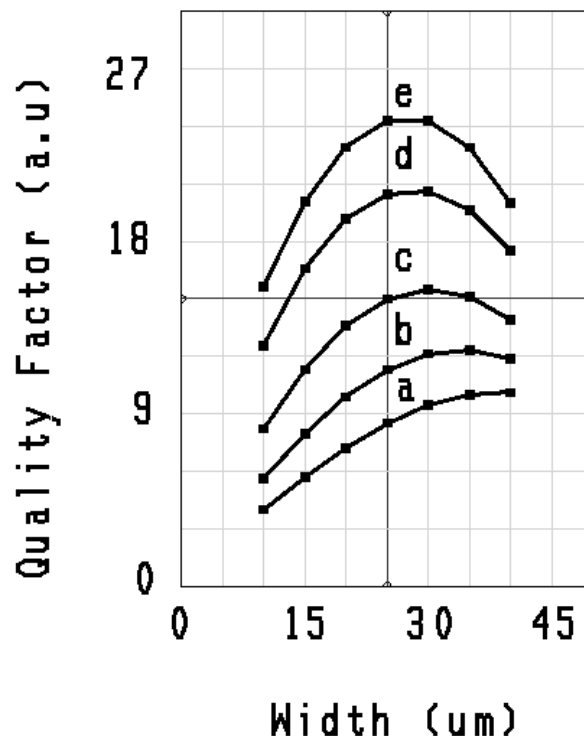


Fig 1. Quality factor as a function of the metal strip width used to perform different 20 nH RF integrated inductors. (a) Shows the quality factors for 0.7 GHz frequency of operation, (b) 1 GHz, (c) 1.5 GHz (d) 2.5 GHz and (e) 3.5 GHz.

To obtain the best set of strip width values we propose an iterative method. First, we define an initial set of values (i.e. the same strip width for all the turns). Then, the magnetic field is calculated across the inductor structure, taking into account any turn to turn interaction. Once the magnetic field is known, ohmic and magnetically induced losses are evaluated for any single

turn of the coil, and the set of strip width values is updated. The process starts again by recalculating the magnetic field for the new geometry, and so on until the desired accuracy is reached.

This procedure has been used to obtain the optimized layout shown on figure 2. The inductor's layout is a 8 turns coil, 30 μm turn to turn spacing, and it has been optimized for a 3.5 GHz frequency of operation. The equivalent inductance is 20 nH.

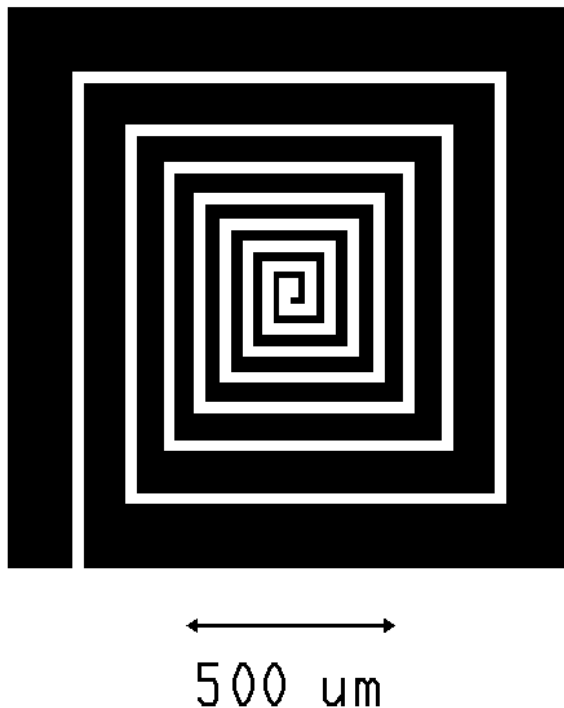


Fig 2. Optimized 20 nH inductor's layout. The optimum frequency of operation is 3.5 GHz.

The performance of this optimized layout is shown on figure 3, where its quality factor is plotted as a function of frequency. On the same figure, the quality factor of other 8 turns, 20 nH inductors are also plotted. Curve (a) corresponds to a 10 μm metal strip width inductor, (b) 25 μm and (c)

40 μm . Curve (d) corresponds to the optimized layout.

As we can see, the optimized inductor shows the best performance in a wide range of frequencies around 3.5 GHz. At this optimum frequency its quality factor is about 1.6 times that of the best single width inductor.

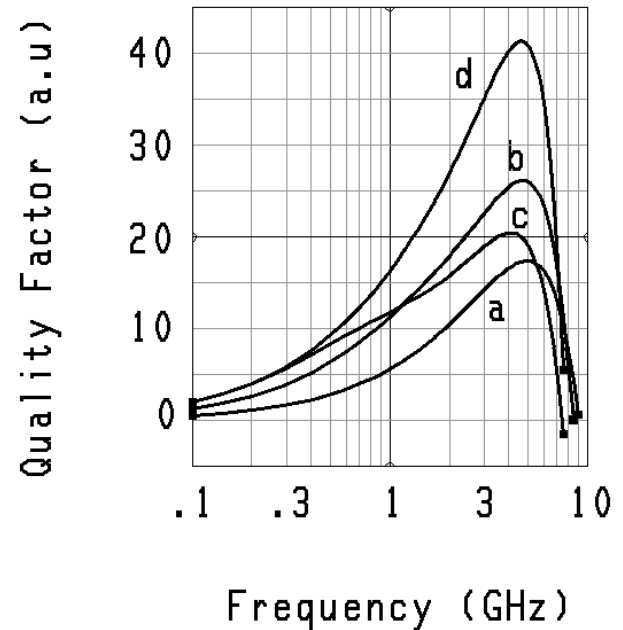


Fig 3. Quality factor as a function of frequency for different 8 turns, 20 nH RF integrated inductors: (a) corresponds to an inductor performed using a metal strip 10 μm wide, (b) 25 μm , (c) 40 μm and (d) optimized layout of figure 2.

CONCLUSION

A method to improve the quality factor of RF integrated inductors by optimizing their layout has been presented. The proposed method has been used to design square spiral inductors in a silicon based MCM technology, complemented with silicon micromachining post processing. The obtained results show that the inductor's layout optimization can increase the quality factor up to a factor 1.6.

REFERENCES

- [1] R.M. Warner and J.N. Fordemwalt (Ed), "*Integrated Circuits Design. Principles and Fabrication*". New York, McGraw-Hill, p267, 1965.
- [2] N.M. Nguyen and R.G. Meyer, "*Si IC compatible inductors and LC passive filters*". IEEE J. Solid-State Circuits, vol 25, pp 1028-1031, Aug. 1990.
- [3] J.Y.C. Chang, A.A. Abidi and M. Gaitan, "*Large Suspended Inductors on Silicon and their use in a 2- μ m CMOS RF Amplifier*". IEEE Electron Dev. Lett., vol 14, pp 246-248, May 1993.
- [4] C.Y. Chi and G.M. Rebeiz, "*Planar Microwave and Millimeter Wave lumped element and coupled line filters using Micromachining Techniques*". IEEE Trans. Microwave Theory Tech., vol 43, pp 730-738, Apr. 1995.
- [5] A. Rofougaran, J.Y.C. Chang, M. Rofougaran and A.A. Abidi, "*A 1 GHz CMOS RF Front-End IC for a Direct Conversion Wireless Receiver*". IEEE J. Solid-State Circuits, vol 31, pp 880-889, July 1996.
- [6] J.Craninckx and S.J. Steyaert, "*A 1.8 GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors*". IEEE J. Solid-State Circuits, vol 32, pp 736-744, May 1997.